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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,498	03/24/2004	David John Butcher	550-541	4617

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,498	BUTCHER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-60 have been considered. Claims 1-16, 31, and 46 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 28 September 2006 and New Drawings as received on 28 September 2006.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 31-60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not describe how it is possible for a computer program product, such as a series of instructions forming a computer program, is able to contain a computer readable storage medium. Since this is not included in the specification, it would be unclear to a person of ordinary skill in the art how to develop this computer program product without undue experimentation.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 31-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear how a computer program product contains a computer readable storage medium.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 6-11, 14-15, 16, 21-26, 29-30, 31, 36-41, 44-45, 46, 51-56, and 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Click, Jr. et al., U.S. Patent Number 6,363,522 (herein referred to as Click) in view of Smith et al., U.S. Patent Number 5,430,862 (herein referred to as Smith).

9. The Examiner notes that, for the purposes of the prior art rejection below for claims 31-60, it is assumed the claims meant to recite "A computer readable storage medium containing a computer program product comprising computer readable instructions for controlling..."

10. Referring to claims 1, 16, and 31, taking claim 1 as exemplary, Click has taught an apparatus for processing data comprising:

a. Wherein said instruction decoder, in response to a memory access instruction,

i. Compares a base register value, stored within a base register specified by a base register field of said memory access instruction, with a predetermined

null value (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7); and,

ii. If said base register value matches said predetermined null value, then said decoder triggers branching to execution of a null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7).

11. Click has not explicitly taught

a. Processing logic operable to perform data processing operations; and

b. An instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions.

12. However, Click has taught that the memory access instructions are executed on a processor, as shown in Figure 5, but provides no details about the "N Processor". Smith has taught

a. Processing logic operable to perform data processing operations (Smith column 2, line 53 to column 4, line 43; Figure 1; and Figure 2); and

b. An instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions (Smith column 2, line 53 to column 4, line 43; Figure 1; and Figure 2).

13. A person of ordinary skill in the art at the time the invention was made, and as taught by Smith, would have recognized that the processor of Smith increases performance and

compatibility by allowing instructions from multiple instruction sets execute (Smith column 1, lines 36-39) and reducing the need to access off-chip memory (Smith column 2, lines 13-24). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the processor of Smith in the device of Click to increase processor performance and compatibility.

14. Claims 16 and 31 have similar limitations to claim 1 and are rejected for similar reasons. The only differences are that claim 16 is for a method and claim 31 is for a computer program product.

15. Referring to claim 46, Click has taught a computer readable medium containing a computer program product comprising a computer program having native program instructions, said native program instructions comprising,

a. In response to memory access instruction decodable by said instruction decoder to control said processing logic:

i. Comparing a base register value stored within a base register specified by a base register field of said memory access instruction with a predetermined null value (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7); and,

ii. If said base register value matches said predetermined null value, then triggering branching to execution of a null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7).

16. Click has not explicitly taught a computer program product including a computer program operable to translate non-native program instructions to form native program instructions directly decodable by an apparatus for processing data having processing logic operable to perform data processing operations and an instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions. However, Click has taught that the memory access instructions are executed on a processor, as shown in Figure 5, but provides no details about the "N Processor". Smith has taught a computer program product including a computer program operable to translate non-native program instructions to form native program instructions directly decodable by an apparatus for processing data having processing logic operable to perform data processing operations and an instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions. (Smith column 2, line 53 to column 4, line 43; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Smith, would have recognized that the processor of Smith increases performance and compatibility by allowing instructions from multiple instruction sets execute (Smith column 1, lines 36-39) and reducing the need to access off-chip memory (Smith column 2, lines 13-24). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the processor of Smith in the device of Click to increase processor performance and compatibility.

17. Referring to claims 6, 21, 36, and 51, taking claim 6 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said null value exception handler is

operable to determine if said memory access instruction attempting to access a location corresponding to a null value corresponds to emulation of a non-native program instruction that is not directly decodable by said instruction decoder attempting to make a memory access using a null value (Click column 1, line 66 to column 2, line 47; column 3, line 48 to column 4, line 7; and column 6, lines 45-67). Claims 21, 36, and 51 have similar limitations to claim 6 and are rejected for similar reasons. The only differences are that claim 21 is for a method and claims 36 and 51 are for a computer program product.

18. Referring to claims 7, 22, 37, and 52, taking claim 7 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said null value exception handler is operable to determine if said memory access instruction attempting to access a location corresponding to a null value corresponds to an error in operation of a virtual machine computer program operable to translate non-native program instructions that are not directly decodable by said instruction decoder into native program instructions that are directly decodable by said instruction decoder (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 22, 37, and 52 have similar limitations to claim 7 and are rejected for similar reasons. The only differences are that claim 22 is for a method and claims 37 and 52 are for a computer program product.

19. Referring to claims 8, 23, 38, and 53, taking claim 8 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 6, wherein said non-native program instructions are machine independent program instructions (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 23, 38, and 53 have similar

limitations to claim 8 and are rejected for similar reasons. The only differences are that claim 23 is for a method and claims 38 and 53 are for a computer program product.

20. Referring to claims 9, 24, 39, and 54, taking claim 9 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 8, wherein said machine independent program instructions are one of:

a. Java bytecodes (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7);

b. MSIL bytecodes;

c. CIL bytecodes; and

d. .NET bytecodes.

21. Claims 24, 39, and 54 have similar limitations to claim 9 and are rejected for similar reasons. The only differences are that claim 24 is for a method and claim 39 and 54 are for a computer program product.

22. Referring to claims 10, 25, 40, and 55, taking claim 10 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 6, wherein said non-native instructions are native program instructions of a different apparatus for processing data (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 25, 40, and 55 have similar limitations to claim 10 and are rejected for similar reasons. The only differences are that claim 25 is for a method and claims 40 and 55 are for a computer program product.

23. Referring to claims 11, 26, 41, and 56, taking claim 11 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 10, wherein said processing logic and said instruction decoder are part of a RISC processor and said non-native instructions are native

instructions of a CISC processor (Smith Abstract; column 1, lines 14-20; column 3, lines 9-20). Claims 26, 41, and 56 have similar limitations to claim 11 and are rejected for similar reasons. The only differences are that claim 26 is for a method and claims 41 and 56 are for a computer program product.

24. Referring to claim 14, 29, 44, and 59, taking claim 14 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said memory access instruction is a load instruction operable to load into a destination register specified by a destination register field within said load instruction a load value dependent upon a value read from a memory location specified by said base register value (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 29, 44, and 59 have similar limitations to claim 14 and are rejected for similar reasons. The only differences are that claim 29 is for a method and claims 44 and 59 are for a computer program product.

25. Referring to claims 15, 30, 45, and 60, taking claim 15 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said memory access instruction is a store instruction operable to store into a memory location specified by said base register value a store value dependent upon source value stored within a source register specified by a source register field within said store instruction (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 30, 45, and 60 have similar limitations to claim 15 and are rejected for similar reasons. The only differences are that claim 30 is for a method and claims 45 and 60 are for a computer program product.

26. Claims 2-5, 12-13, 17-20, 27-28, 32-35, 42-43, 47-50, and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Click, Jr. et al., U.S. Patent Number 6,363,522 (herein

referred to as Click) in view of Smith et al., U.S. Patent Number 5,430,862 (herein referred to as Smith) as applied to claims 1, 16, 32, and 46 above, and further in view of Mirapuri et al., U.S. Patent Number 5,590,294 (herein referred to as Mirapuri).

27. Referring to claims 2, 17, 32, and 47, taking claim 2 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, but not taught wherein in response to said memory access instruction a return address is stored pointing a memory location storing a program instruction to be executed upon a return from said null value exception handler. Mirapuri has taught wherein in response to said memory access instruction a return address is stored pointing a memory location storing a program instruction to be executed upon a return from said null value exception handler (Mirapuri column 2, lines 41-51; column 7, lines 36-53; column 10, lines 15-41; column 12, line 53 to column 13, line 10; and Figure 8). A person of ordinary skill in the art at the time the invention was made, and as taught by Mirapuri, the device of Mirapuri improves pipeline throughput (Mirapuri column 3, lines 3-5), thereby improving processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the co-processing of Mirapuri in the device of Smith to improve processor efficiency and speed. Claims 17, 32, and 47 have similar limitations to claim 2 and are rejected for similar reasons. The only differences are that claim 17 is for a method and claims 32 and 47 are for a computer program product.

28. Referring to claims 3, 18, 33, and 48, taking claim 3 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 1, wherein said null value exception handler is located at a memory address pointed to by a value stored within a programmable configuration register (Mirapuri column 2, lines 41-51; column 7, lines

36-53; column 10, lines 15-41; column 12, line 53 to column 13, line 10; and Figure 8). Claims 18, 33, and 48 have similar limitations to claim 3 and are rejected for similar reasons. The only differences are that claim 18 is for a method and claims 33 and 48 are for a computer program product.

29. Referring to claims 4, 19, 34, and 49, taking claim 4 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said programmable configuration register is a coprocessor configuration register (Mirapuri column 2, lines 41-51; column 7, lines 36-53; column 10, lines 15-41; column 12, line 53 to column 13, line 10; and Figure 8). Claims 19, 34, and 49 have similar limitations to claim 19 and are rejected for similar reasons. The only differences are that claim 19 is for a method and claims 34 and 49 are for a computer program product.

30. Referring to claims 5, 20, 35, and 50, taking claim 5 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said branch is made to an instruction stored at a memory address given by said value stored within said programmable configuration register subject to a fixed offset (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 20, 35, and 50 have similar limitations to claim 5 and are rejected for similar reasons. The only differences are that claim 20 is for a method and claims 35 and 50 are for a computer program product.

31. Referring to claims 12, 27, 42, and 57, taking claim 12 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said value stored within said programmable configuration register is a start address of said null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to

column 4, line 7). Claims 27, 42, and 57 have similar limitations to claim 12 and are rejected for similar reasons. The only differences are that claim 12 is for a method and claims 42 and 57 are for a computer program product.

32. Referring to claims 13, 28, 43, and 58, taking claim 13 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said value stored within said programmable configuration register is an address of a jump instruction operable to jump execution to a start address of said null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 28, 43, and 58 have similar limitations to claim 13 and are rejected for similar reasons. The only differences are that claim 13 is for a method and claims 43 and 58 are for a computer program product.

Response to Arguments

33. Examiner withdraws the drawing objections in favor of the replacement drawings.

34. Examiner withdraws claim objections in favor of the amended claims.

35. Examiner withdraws the rejection of claims 31-60 under 35 USC §101 in favor of the amended claims.

36. Applicant's arguments filed 28 September 2006 have been fully considered but they are not persuasive.

37. Applicants argue in essence on pages 18-20 and 21

> ...Examiner does not include any allegation that either primary reference Click or secondary reference Smith teach both (A) any hardware which accomplishes the base register value comparison with the predetermined null value; and (B)

triggering branching to execution of a null value exception handler. Should the Examiner believe either the Click or Smith reference contain any disclosure which could vaguely be considered suggestive of Applicants' claimed hardware (instruction decoder), she is respectfully requested to identify such structure...

38. This has not been found persuasive. The decoder in the claim language is found within the combined references. The claim language merely recites "an instruction decoder to decode program instructions to control said processing logic...in response to a memory access instruction, compares a base register value...with a predetermined null value; and...said decoder triggers branching to execution of a null value exception handler." As shown in the previous rejection and the rejection above, Click has taught the functionality with the predetermined null value and that the memory access instruction and associated instructions are performed in a processor (Click Figure 5). Smith was relied upon to teach the details of the processor in Click's Figure 5. As shown by Smith in Figure 2; column 2, line 63 to column 3, line 8; and column 3, lines 41-45, there is a decoder in the processor that decodes instructions and triggers a branch to another routine. In this case, the routine would be that taught by Click. The decoder of Smith decodes each instruction it receives to determine what operation the processor performs. In this case the decoder of Smith receives the instructions of Click to determine what operations are to be run. Applicant's arguments seem to suggest that the claim language explicitly states that the decoder performs all the functions described in the claim when it only receives a memory access instruction. However, the claim language has open claim language and the decoder can receive other instructions to perform the null exception handling, as taught by Click, as long as it performs the functions in response to the memory access instruction. Click has taught that

subsequent instructions issued for the null exception handler are in response to the memory access instruction and the processor's decoder of Smith decodes these instructions so the proper operations are executed, e.g. triggering the operations, including the branching, to be executed. Also, whether the functionality is done in hardware or software is irrelevant. Andres S. Tannenbaum's Structured Computer Organization Second Edition © 1984 has taught that what is done in software can be done in hardware and vice versa. It is a design choice based upon the advantages of each method. So, the fact that the functionality described in the claims is in software, as in Click, or hardware, as argued by Applicant, is irrelevant. The advantages argued in Applicants' arguments is mere allegation at this point. Without proof of unexpected results that must be supplied in an affidavit, the arguments will continue to be mere allegation. There is also no language in claims as to how the hardware that performs all the functionality is physically different from other decoders that do not perform these functions.

39. Applicants argue in essence on pages 20-22 "...Examiner has provided no 'reason' or 'motivation' for combining Click, Smith, and Mirapuri references..." This has not been found persuasive. As show in the previous rejection and the rejection above, Smith teaches, in column 1, lines 36-39, that his specific processor design increases compatibility and, in column 2, lines 13-24, improves performance. Also, Mirapuri teaches in column 3, lines 3-5 that his device improves pipeline throughput. When pipeline throughput is improved, i.e. more instructions are executed by the pipeline, processor efficiency and speed is improved since there are less idle cycles wasting time and resources.

40. In addition, Applicants argue in essence on pages 20-22 "...The Examiner also has ignored the fact that Click's teaching of using software for null value checking specifically

teaches away from locating null value checking in hardware as claimed..." This has not been found persuasive. As stated in the above remarks with regard to the hardware vs. software implementation, this is a design choice (Tanenbaum pages 10-12). Also, there is nowhere in Click that states the functionality described in their specification and in the instant application's claims cannot be implemented in hardware nor that, if the functionality described were implemented in hardware, then it would not function properly. The Examiner is unclear as to how Click teaches away from implementing the functionality described and claimed in hardware.

Conclusion

41. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

42. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
6 December 2006

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